International J. of Multidispl.Research & Advcs. in Engg.(IJMRAE),
ISSN 0975-7074, Vol. 9, No. III (December 2017), pp 55-62

C-V CHARACTERIZATION OF MOS IN THE PRESENCE OF HCL FOR OXIDATION PROCESS

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Abstract

In the proposed paper C-V characterization of MOS fabricated in HCl environment at the time of oxidation is studied. To establish a comparative result, the C-V characterization of MOS without HCl at the time of oxidation is also studied and the final results are presented which are helpful in bulk micromachining of silicon.

Key words: MOS, C-V measurement, Silicon, Oxidation, Micromachining.

1. INTRODUCTION

Capacitance –Voltage measurement of MOS capacitors is a rich source of information about the structure, which is of direct interest when one evaluates the MOS process. Since the MOS structure is simple to fabricate, the technique is widely used. To understand capacitance-voltage measurement one must first be familiar with the frequency dependence of the measurement. This frequency dependence occurs primarily in inversion since certain amount of time is needed to generate the minority carriers in the inversion layer [1]. Thermal equilibrium is, therefore, not immediately obtained.

The low frequency or quasi-static measurement maintains thermal equilibrium at all times. The capacitance observed in this condition is the ratio of the change in charge to the change in gate voltage; measurements are made while the capacitor is in equilibrium [2]. A typical measurement is performed with an electrometer, which measures the charge added per unit time as the applied gate voltage is slowly varied [3].

The high frequency capacitance is obtained from a small signal capacitance measurement at high frequency. The bias voltage on the gate is varied slowly to obtain the capacitance versus voltage characteristics. Under such condition, the charge in the inversion layer does not change from the equilibrium value at the applied dc voltage. The high frequency capacitance, therefore, reflects only the charge variation in the depletion layer or rather the small movement of the inversion layer change [4].

In the next section the simple capacitance model is derived which is based on the full depletion approximation including our basic assumptions. The comparison with the exact low frequency capacitance will reveal that the largest error occurs at the flat band voltage. The exact flat band capacitance is derived using the linearized Poisson's equation [5].

2. SIMPLE CAPACITANCE MODEL

The MOS structure is treated as a series connection of two capacitors: the capacitance of the oxide and the capacitance of the depletion layer. In accumulation, there is no depletion layer. The remaining capacitor is because of the oxide capacitance. Thus, the capacitance equals:

$$C_{LF} = C_{HF} = C_{ox} \quad ; \text{ for } V_G \leq V_{FB} \tag{1}$$

In depletion, the MOS capacitance is obtained from the series connection of the oxide capacitance and the depletion layer capacitance.

$$C_{LF} = C_{HF} = \frac{1}{\frac{1}{C_{ox}} + \frac{x_d}{\varepsilon_s}} \quad ; \text{ for } V_{FB} \leq V_G \leq V_T \tag{2}$$

Where x_d is the variable depletion layer width which is obtained from:

$$x_d = \sqrt{\frac{2\varepsilon_s \Phi_s}{qN_d}} \tag{3}$$

In order to obtain the capacitance corresponding to a specific value of the gate voltage; the relation between the potential across the depletion region and the gate voltage is used, which is given as [6]:

$$V_G = V_{FB} + \Phi_s + \sqrt{\frac{2\varepsilon_s q N_a \Phi_s}{C_{ox}}} \quad ; \text{ for } \quad 0 \leq \Phi_s \leq \ 2\Phi_F \tag{4}$$

In inversion, the capacitance becomes independent of the gate voltage [7]. The low frequency capacitance equals the oxide capacitance since charges are added to and removed from the inversion layer. The high frequency capacitance is obtained from the series connection of the oxide capacitance and the capacitance of the depletion layer having its maximum width, X_{dT} .The capacitances are given by:

$$C_{LF} = C_{ox} \text{ and } C_{HF} = \frac{1}{\frac{1}{C_{ox}}+\frac{x_{dT}}{\varepsilon_s}} \;;\; \text{for } V_G \geq V_T \quad (5)$$

3. FLAT BAND CAPACITANCE

To obtain the actual flat band capacitance, the Poisson's equation is first linearized. Since the potential across the semiconductor at flat band is zero, we expect the potential to be small as we very the gate voltage around the flat band voltage. Poisson's equation can, thus, be simplified to [8]:

$$\frac{d^2\Phi}{dx^2} = \frac{q}{\varepsilon_s}(N_a^+ - p) = \frac{qN_a}{\varepsilon_s}\left(1 - e^{\frac{-\Phi}{V_T}}\right) \quad (6)$$

$$\approx \frac{qN_a\Phi}{\varepsilon_s V_t} \quad (7)$$

The solution of this equation is:

$$\varphi = \varphi_s e^{-\frac{x}{L_D}} \;, \quad \text{with} \quad L_D = \sqrt{\frac{\varepsilon_s V_t}{qN_a}} \quad (8)$$

Where, Φ_s is the potential at the surface of the semiconductor and L_D is the Debye length. The solution of the potential enables the derivation of the capacitance of the semiconductor under flat band condition; thus:

$$C_{S_{FB}} = \frac{d\theta_s}{d\Phi_s} = \frac{d\left(\varepsilon_s \cdot \frac{\Phi_s}{L_D}\right)}{d\Phi_s} = \frac{\varepsilon_s}{L_D} \quad (9)$$

The flat band capacitance of the MOS structure is obtained by calculating the series connection of the oxide capacitor and the capacitance of the semiconductor:

$$C_{FB} = \frac{1}{\frac{1}{C_{ox}}+\frac{L_d}{\varepsilon_s}} \quad (10)$$

4. DEEP DEPLETION CAPACITANCE

Deep depletion occurs in MOS capacitor when measuring the high – frequency capacitance while sweeping the gate voltage "quickly". Quickly means that the gate voltage must be changed fast enough so that the structure could not attain the thermal equilibrium.

When ramping the voltage from flat band to threshold and beyond, the inversion layer is not or only partially formed. This occurs since the generation of minority carriers cannot keep up with the amount needed to from the full inversion layer. The depletion layer, therefore, keeps increasing beyond its maximum thermal equilibrium value, X_{dT}; resulting in a capacitance which further decreases with voltage [9,10].

5. EXPERIMENTAL CALCULATION OF C-V MEASUREMENT

For a MOS capacitor system with p-type Si substrate having resistivity 30-50 Ω.cm and the thickness of SiO_2 layer is 0.1μm.

5.1 Doping Density of Acceptor Atoms

Resistivity of p- type substrate $\rho_p = 30$ Ω.cm

Mobility of hole μ_P =500 cm^2 N-s

Electronic charge $q = 1.6 \times 10^{-19}$ C

We know that,

$\rho_p = 1/ (N_A \times q \times \mu_p)$ i.e. $30 = 1/ (N_A \times 1.6 \times 10^{-19} \times 500)$

$N_A = 2.08 \times 10^{15}$ $/cm^3$

5.2 The Bulk Potential of the MOS System

Doping density of acceptor atom $N_A = 2.08 \times 10^{15}$ $/cm^3$

Density of change in intrinsic Si , $n_i = 1.5 \times 10^{10}$ $/cm^3$

We know that,

$$\Phi_F = \frac{KT}{q} \ln \left(\frac{N_a}{n_i}\right) = 0.0259 \ln \left(\frac{2.08\times10^{15}}{1.5\times10^{10}}\right) = 0.306 \text{ V}$$

5.3 Width of Depletion Region

Permittivity of Si, $\varepsilon_s = 11.8 \times 8.85 \times 10^{-14}$ F/cm

Bulk potential of MOS system, Φ_F =0.265 V

Electronic charge $q = 1.6 \times 10^{-19}$ C

$N_A = 2.08 \times 10^{15}$ $/cm^3$

We know that,

$$W_{max} = \sqrt{\frac{2\varepsilon_s \Phi_s(inv)}{qN_A}} = \sqrt{\frac{4\varepsilon_s kT \ln(\frac{N_A}{n_i})}{q^2 N_A}} = 0.6197 \text{ μm}$$

5.4 Insulator Capacitance

Permittivity of the insulating layer (SiO2), $\varepsilon_i = 3.9\times8.85\times10^{-14}$ F/cm

Insulator thickness, d = 0.1 µm

We know that,

$C_i = \varepsilon_i A / d$

$A = (250)^2 \times (10^{-4})^2 \times 3.14 = 1.96\times10^{-3}$ cm^2

$C_i = (3.9 \times 8.85 \times 10^{-14} \times 1.96 \times 10^{-13}) / (0.1 \times 10^{-4})$

$C_i =$ 67.77 pF

5.5 Charge Per unit Area in the Depletion Region at Strong Inversion

Electronic charge $q = 1.6 \times10^{-19}$ c

Doping density of acceptor atom, $N_A = 2.08\times10^{15}$ /cm^3

Width of the depletion region, $W_M = 1.289$ µm

We know that,

$Q_d = -qN_AW_M = -2.062 \times 10^{-8}$ C/cm^2

5.6 Threshold Voltage

Charge per unit area in the depletion region at strong inversion

$Q_d = -2.062 \times 10^{-8}$ C/cm^2

Insulator capacitance, $C_i = 0.034$ pF = 34.515 nF/cm^2

The bulk potential of the MOS system $\Phi_F = 0.306$ V

We know that,

$$V_T = -\frac{Q_d}{C_i} + 2\Phi_F = 1.209 \text{ V}$$

5.7 Depletion Layer Capacitance at Maximum Depletion

Permittivity of Si, $\varepsilon_s = 11.8\times8.85\times10^{-14}$ F/cm

Width of the depletion region, W = 0.6197 µm

We know that,

$C_d = \varepsilon_s / W_M = 16.851$ pF/cm^2

5.8 Total Capacitance at Maximum Depletion

$$C = \frac{C_i C_D}{C_i + C_D} = 11.32 \text{ pF /cm}^2$$

6. CV MEASUREMENT:-

After C-V measurement, a plot between capacitance and voltage with and without HCL and is shown in figure 1 and 2 respectively.

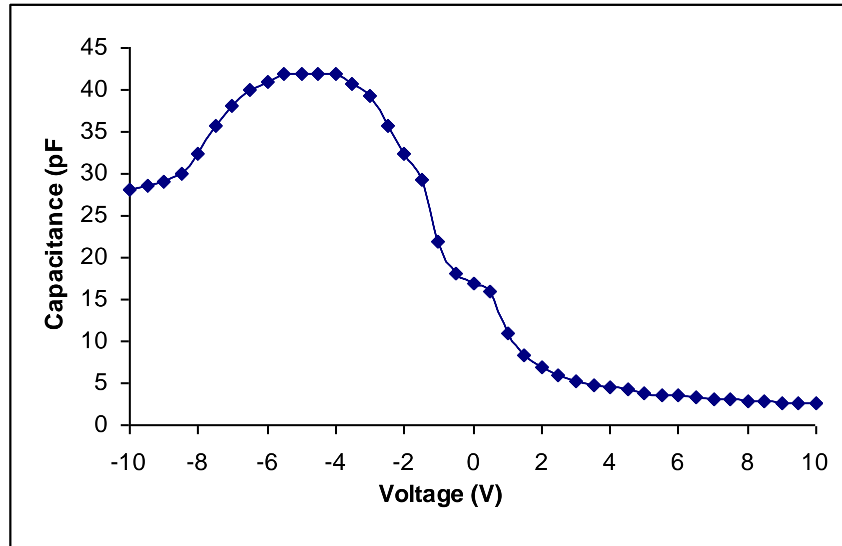

Fig 1: C-V plot without HCl

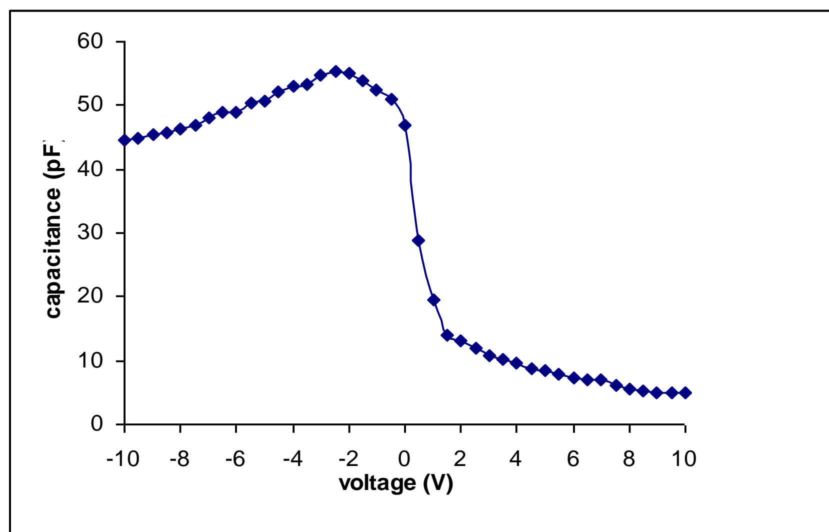

Fig 2: C-V plot with HCl

7. RESULTS

In the calculation of CV measurement, it is obtained that

Doping density of acceptor atom, $N_A = 2.08 \times 10^{15}$ /cm^3

The bulk potential of the MOS system: $\Phi_F = 0.306$ V

Width of the depletion region, $W_M = 0.6197$ μm

Insulator Capacitance: $C_i = 67.77$ pF

Change per unit area in the depletion region at string in version:

$$Q_d == -2.062 \times 10^{-8} \text{ C/cm}^2$$

Threshold voltage: $V_T = 1.209$ V

Depletion layer capacitance at maximum depletion: $C_d = 16.851$ pF /cm^2

Total capacitance at maximum depletion: $C_{min} = 11.32$ pF

CONCLUSION

In the study and design of the MOS fabrication and C-V measurement together with fabrication of p-n junction diode, it is observed that if HCl is introduced during oxidation step; it results into drastic reduction of leakage current; besides this an improvement in breakdown voltage is also observed.

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